Cost-Optimized Portfolio
Product Tables and Product Selection Guide

SPARTAN 6 SPARTAN 7 ARTIX 7 ZYNQ CoolRunner-II

XILINX
ALL PROGRAMMABLE™

Zynq®-7000 AP SoC Family

		Cost-Optimized Devices						Mid-Range Devices			
	Device Name	Z-7007S	Z-7012S	Z-7014S	Z-7010	Z-7015	Z-7020	Z-7030	Z-7035	Z-7045	Z-7100
	Part Number	XC7Z007S	XC7Z012S	XC7Z014S	XC7Z010	XC7Z015	XC7Z020	XC7Z030	XC7Z035	XC7Z045	XC7Z100
Processing System (PS)	Processor Core	Single-Core ARM® Cortex™-A9 MPCore™ Up to 766MHz			Dual-Core ARM Cortex-A9 MPCore Up to 866MHz			Dual-Core ARM Cortex-A9 MPCore Up to 1GHz[1]			
	Processor Extensions	NEON™ SIMD Engine and Single/Double Precision Floating Point Unit per processor									
	L1 Cache	32KB Instruction, 32KB Data per processor									
	L2 Cache	512KB									
	On-Chip Memory	256KB									
	External Memory Support[2]	DDR3, DDR3L, DDR2, LPDDR2									
	External Static Memory Support[2]	2x Quad-SPI, NAND, NOR									
	DMA Channels	8 (4 dedicated to PL)									
	Peripherals	2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO									
	Peripherals w/ built-in DMA[2]	2x USB 2.0 (OTG), 2x Tri-mode Gigabit Ethernet, 2x SD/SDIO									
	Security[3]	RSA Authentication of First Stage Boot Loader, AES and SHA 256b Decryption and Authentication for Secure Boot									
	Processing System to Programmable Logic Interface Ports (Primary Interfaces & Interrupts Only)	2x AXI 32b Master, 2x AXI 32b Slave 4x AXI 64b/32b Memory AXI 64b ACP 16 Interrupts									
Programmable Logic (PL)	7 Series PL Equivalent	Artix®-7	Artix-7	Artix-7	Artix-7	Artix-7	Artix-7	Kintex®-7	Kintex-7	Kintex-7	Kintex-7
	Logic Cells	23K	55K	65K	28K	74K	85K	125K	275K	350K	444K
	Look-Up Tables (LUTs)	14,400	34,400	40,600	17,600	46,200	53,200	78,600	171,900	218,600	277,400
	Flip-Flops	28,800	68,800	81,200	35,200	92,400	106,400	157,200	343,800	437,200	554,800
	Total Block RAM (# 36Kb Blocks)	1.8Mb (50)	2.5Mb (72)	3.8Mb (107)	2.1Mb (60)	3.3Mb (95)	4.9Mb (140)	9.3Mb (265)	17.6Mb (500)	19.2Mb (545)	26.5Mb (755)
	DSP Slices	66	120	170	80	160	220	400	900	900	2,020
	PCI Express®	—	Gen2 x4	—	—	Gen2 x4	—	Gen2 x4	Gen2 x8	Gen2 x8	Gen2 x8
	Analog Mixed Signal (AMS) / XADC[2]	2x 12 bit, MSPS ADCs with up to 17 Differential Inputs									
	Security[3]	AES & SHA 256b Decryption & Authentication for Secure Programmable Logic Config									
	Speed Grades: Commercial	-1			-1			-1			-1
	Speed Grades: Extended	-2			-2,-3			-2,-3			-2
	Speed Grades: Industrial	-1, -2			-1, -2, -1L			-1, -2, -2L			-1, -2, -2L

Notes:
1. 1 GHz processor frequency is available only for -3 speed grades for devices in flip-chip packages. Please see the data sheet for more details.
2. Z-7007S and Z-7010 in CLG225 have restrictions on PS peripherals, memory interfaces, and I/Os. Please refer to the Technical Reference Manual for more details.
3. Security block is shared by the Processing System and the Programmable Logic.

Zynq®-7000 All Programmable SoC Family
HR I/O, HP I/O, PS I/O, and Transceivers (GTP or GTX)

			Cost-Optimized Devices						Mid-Range Devices			
		Device Name	Z-7007S	Z-7012S	Z-7014S	Z-7010	Z-7015	Z-7020	Z-7030	Z-7035	Z-7045	Z-7100
Package Footprint	Dimensions (mm) [1]	Ball Pitch (mm)	HR I/O, HP I/O PS I/O[2], GTP Transceivers						HR I/O, HP I/O PS I/O[2], GTX Transceivers			
CLG225	13x13	0.8	54, 0 84[3], 0			54, 0 84[3], 0						
CLG400	17x17	0.8	100, 0 128, 0		125, 0 128, 0	100, 0 128, 0		125, 0 128, 0				
CLG484	19x19	0.8			200, 0 128, 0			200, 0 128, 0				
CLG485[4]	19x19	0.8		150, 0 128, 4			150, 0 128, 4					
SBG485[4]	19x19	0.8							50, 100 128, 4			
FBG484	23x23	1.0							100, 63 128, 4			
FBG676[1]	27x27	1.0							100, 150 128, 4	100, 150 128, 8	100, 150 128, 8	
FFG676[1]	27x27	1.0							100, 150 128, 4	100, 150 128, 8	100, 150 128, 8	
FFG900	31x31	1.0								212, 150 128, 16	212, 150 128, 16	212, 150 128, 16
FFG1156	35x35	1.0										250, 150 128, 16

Notes:
1. Devices in the same package are footprint compatible. FBG676 and FFG676 are also footprint compatible.
2. PS I/O count does not include dedicated DDR calibration pins.
3. PS DDR and PS MIO pin count is limited by package size. See DS190, *Zynq-7000 All Programmable SoC Overview* for details.
4. CLG485 and SBG485 are pin-to-pin compatible. See product data sheets and user guides for more details.
   See DS190, *Zynq-7000 All Programmable SoC Overview* for package details.

Artix-7 FPGAs

		Transceiver Optimization at the Lowest Cost and Highest DSP Bandwidth (1.0V, 0.95V, 0.9V)							
	Part Number	XC7A12T	XC7A15T	XC7A25T	XC7A35T	XC7A50T	XC7A75T	XC7A100T	XC7A200T
Logic Resources	Logic Cells	12,800	16,640	23,360	33,280	52,160	75,520	101,440	215,360
	Slices	2,000	2,600	3,650	5,200	8,150	11,800	15,850	33,650
	CLB Flip-Flops	16,000	20,800	29,200	41,600	65,200	94,400	126,800	269,200
Memory Resources	Maximum Distributed RAM (Kb)	171	200	313	400	600	892	1,188	2,888
	Block RAM/FIFO w/ ECC (36 Kb each)	20	25	45	50	75	105	135	365
	Total Block RAM (Kb)	720	900	1,620	1,800	2,700	3,780	4,860	13,140
Clock Resources	CMTs (1 MMCM + 1 PLL)	3	5	3	5	5	6	6	10
I/O Resources	Maximum Single-Ended I/O	150	250	150	250	250	300	300	500
	Maximum Differential I/O Pairs	72	120	72	120	120	144	144	240
Embedded Hard IP Resources	DSP Slices	40	45	80	90	120	180	240	740
	PCIe® Gen2[1]	1	1	1	1	1	1	1	1
	Analog Mixed Signal (AMS) / XADC	1	1	1	1	1	1	1	1
	Configuration AES / HMAC Blocks	1	1	1	1	1	1	1	1
	GTP Transceivers (6.6 Gb/s Max Rate)[2]	2	4	4	4	4	8	8	16
Speed Grades	Commercial Temp (C)	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2
	Extended Temp (E)	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3
	Industrial Temp (I)	-1, -2, -1L	-1, -2, -1L	-1, -2, -1L	-1, -2, -1L	-1, -2, -1L	-1, -2, -1L	-1, -2, -1L	-1, -2, -1L

	Package[3, 4]	Dimensions (mm)	Ball Pitch (mm)	**Available User I/O**: 3.3V SelectIO™ HR I/O (GTP Transceivers)							
	CPG236	10 x 10	0.5		106 (2)		106 (2)	106 (2)			
	CPG238	10 x 10	0.5	112 (2)		112 (2)					
	CSG324	15 x 15	0.8		210 (0)		210 (0)	210 (0)	210 (0)	210 (0)	
	CSG325	15 x 15	0.8	150 (2)	150 (4)	150 (4)	150 (4)	150 (4)			
	FTG256	17 x 17	1.0		170 (0)		170 (0)	170 (0)	170 (0)	170 (0)	
	SBG484	19 x 19	0.8								285 (4)
Footprint Compatible	FGG484[5]	23 x 23	1.0		250 (4)		250 (4)	250 (4)	285 (4)	285 (4)	
	FBG484[5]	23 x 23	1.0								285 (4)
Footprint Compatible	FGG676[6]	27 x 27	1.0						300 (8)	300 (8)	
	FBG676[6]	27 x 27	1.0								400 (8)
	FFG1156	35 x 35	1.0								500 (16)

Notes:
1. Supports PCI Express Base 2.1 specification at Gen1 and Gen2 data rates.
2. Represents the maximum number of transceivers available. Note that the majority of devices are available without transceivers. See the Package section of this table for details.
3. Leaded package option available for all packages. See DS180, *7 Series FPGAs Overview* for package details.
4. Device migration is available within the Artix-7 family for like packages but is not supported between other 7 series families.
5. Devices in FGG484 and FBG484 are footprint compatible.
6. Devices in FGG676 and FBG676 are footprint compatible.

Spartan-7 FPGAs

		I/O Optimization at the Lowest Cost and Highest Performance-per-Watt (1.0V, 0.95V)					
	Part Number	**XC7S6**	**XC7S15**	**XC7S25**	**XC7S50**	**XC7S75**	**XC7S100**
Logic Resources	Logic Cells	6,000	12,800	23,360	52,160	76,800	102,400
	Slices	938	2,000	3,650	8,150	12,000	16,000
	CLB Flip-Flops	7,500	16,000	29,200	65,200	96,000	128,000
Memory Resources	Max. Distributed RAM (Kb)	70	150	313	600	832	1,100
	Block RAM/FIFO w/ ECC (36 Kb each)	5	10	45	75	90	120
	Total Block RAM (Kb)	180	360	1,620	2,700	3,240	4,320
Clock Resources	Clock Mgmt Tiles (1 MMCM + 1 PLL)	2	2	3	5	8	8
I/O Resources	Max. Single-Ended I/O Pins	100	100	150	250	400	400
	Max. Differential I/O Pairs	48	48	72	120	192	192
Embedded Hard IP Resources	DSP Slices	10	20	80	120	140	160
	Analog Mixed Signal (AMS) / XADC	0	0	1	1	1	1
	Configuration AES / HMAC Blocks	0	0	1	1	1	1
Speed Grades	Commercial Temp (C)	-1,-2	-1,-2	-1,-2	-1,-2	-1,-2	-1,-2
	Industrial Temp (I)	-1,-2,-1L	-1,-2,-1L	-1,-2,-1L	-1,-2,-1L	-1,-2,-1L	-1,-2,-1L
	Expanded Temp (Q)	-1	-1	-1	-1	-1	-1

Package[1]	Body Area (mm)	Ball Pitch (mm)	**Available User I/O**: 3.3V SelectIO™ HR I/O					
CPGA196	8x8	0.5	100	100				
CSGA225	13x13	0.8	100	100	150			
CSGA324	15x15	0.8			150	210		
FTGB196	15x15	1.0	100	100	100	100		
FGGA484	23x23	1.0				250	338	338
FGGA676	27x27	1.0					400	400

1. Packages with the same last letter and number sequence, e.g., A484, are footprint compatible with all other Spartan-7 devices with the same sequence. The footprint compatible devices within this family are outlined.

Spartan-6 FPGAs

			Spartan®-6 LX FPGAs I/O Optimization at the Lowest Cost (1.2V, 1.0V)							Spartan-6 LXT FPGAs I/O Optimization at the Lowest-Cost with Serial Connectivity (1.2V)				
Part Number			XC6SLX4	XC6SLX9	XC6SLX16	XC6SLX25	XC6SLX45	XC6SLX75	XC6SLX100	XC6SLX150	XC6SLX25T	XC6SLX45T	XC6SLX75T	XC6SLX100T	XC6SLX150T
Slices[1]			600	1,430	2,278	3,758	6,822	11,662	15,822	23,038	3,758	6,822	11,662	15,822	23,038
Logic Cells[2]			3,840	9,152	14,579	24,051	43,661	74,637	101,261	147,443	24,051	43,661	74,637	101,261	147,443
CLB Flip-Flops			4,800	11,440	18,224	30,064	54,576	93,296	126,576	184,304	30,064	54,576	93,296	126,576	184,304
Max. Distributed RAM (Kb)			75	90	136	229	401	692	976	1,355	229	401	692	976	1,355
Block RAM (18Kb each)			12	32	32	52	116	172	268	268	52	116	172	268	268
Total Block RAM (Kb)[3]			216	576	576	936	2,088	3,096	4,824	4,824	936	2,088	3,096	4,824	4,824
Clock Mgmt Tiles (CMT)[4]			2	2	2	2	4	6	6	6	2	4	6	6	6
Max. Single-Ended I/O Pins			132	200	232	266	358	408	480	576	250	296	348	498	540
Max. Differential I/O Pairs			66	100	116	133	179	204	240	288	125	148	174	249	270
DSP48A1 Slices[5]			8	16	32	38	58	132	180	180	38	58	132	180	180
Endpoint Block for PCIe®			—	—	—	—	—	—	—	—	1	1	1	1	1
Memory Controller Blocks			0	2	2	2	2	4	4	4	2	2	4	4	4
GTP Low-Power Transceivers			—	—	—	—	—	—	—	—	2	4	8	8	8
Commercial Speed Grade[10]			-1L, -2, -3	-1L, -2, -3, -3N	-1L, -2, -3, -3N	-1L, -2, -3, -3N	-1L, -2, -3, -3N	-1L, -2, -3, -3N	-1L, -2, -3, -3N	-1L, -2, -3, -3N	-2, -3, -3N	-2, -3, -3N	-2, -3, -3N	-2, -3, -3N	-2, -3, -3N
Industrial Speed Grade[10]			-1L, -2, -3	-1L, -2, -3, -3N	-1L, -2, -3, -3N	-1L, -2, -3, -3N	-1L, -2, -3, -3N	-1L, -2, -3, -3N	-1L, -2, -3, -3N	-1L, -2, -3, -3N	-2, -3, -3N	-2, -3, -3N	-2, -3, -3N	-2, -3, -3N	-2, -3, -3N
Configuration Memory (Mb)			2.7	2.7	3.7	6.4	11.9	19.6	26.5	33.8	6.4	11.9	19.6	26.5	33.8
Package	Body Area (mm)	Ball Pitch (mm)	**Maximum User I/O**: SelectIO™ Interface Pins (GTP Transceivers)[6]												
CPG196[7]	8 x 8	0.5	106	106	106										
TQG144[7]	20 x 20	0.5	102	102											
CSG225[8]	13 x 13	0.8	132	160	160										
CSG324	15 x 15	0.8		200	232	226	218				190 (2)	190 (4)			
CSG484[9]	19 x 19	0.8					320	328	338	338		296 (4)	292 (4)	296 (4)	296 (4)
FT(G)256	17 x 17	1.0		186	186	186									
FG(G)484[9]	23 x 23	1.0				266	316	280	326	338	250 (2)	296 (4)	268 (4)	296 (4)	296 (4)
FG(G)676	27 x 27	1.0					358	408	480	498			348 (8)	376 (8)	396 (8)
FG(G)900	31 x 31	1.0								576				498 (8)	540 (8)

Notes:
1. Each slice contains four LUTs and eight flip-flops.
2. Spartan-6 FPGA logic cell ratings reflect the increased logic capacity offered by the 6-input LUT architecture.
3. Block RAM are fundamentally 18Kb in size. Each block can also be used as two independent 9 Kb blocks.
4. Each CMT contains two DCMs and one PLL.
5. Each DSP48A1 slice contains an 18x18 multiplier, an adder, and an accumulator.
6. The LX device pinouts are not compatible with the LXT device pinouts.
7. CPG196 and TQG144 do not have memory controller support. -3N is not available for these packages.
8. CSG225 has X8 memory controller support in the LX9 and LX16 devices. There is no memory controller in the LX4 devices.
9. Devices in the FG(G)484 and CSG484 packages have support for two memory controllers.
10. Devices with -3N speed grade do not support MCB functionality.

CoolRunner-II CPLDs

		High performance and ultra-low power consumption in a single-chip, instant-on programmable device (1.8V)					
	Part Number	XC2C32A	XC2C64A	XC2C128	XC2C256	XC2C384	XC2C512
Logic Resources	System Gates	750	1,500	3,000	6,000	9,000	12,000
	Macrocells	32	64	128	256	384	512
	Product Terms Per Macrocell	56	56	56	56	56	56
Clock Resources	Global Clocks	3	3	3	3	3	3
	Product Term Clocks Per Function Block	16	16	16	16	16	16
I/O Resources	Maximum I/O	33	64	100	184	240	270
	Input Voltage Compatible	1.5 / 1.8 / 2.5 / 3.3					
	Output Voltage Compatible	1.5 / 1.8 / 2.5 / 3.3					
Speed Grades	Min. Pin-to-Pin Logic Delay (ns)	3.8	4.6	5.7	5.7	7.1	7.1
	Commercial Speed Grades (Fastest to Slowest)	-4, -6	-5, -7	-6, -7	-6, -7	-7, -10	-7, -10
	Industrial Speed Grades (Fastest to Slowest)	-6	-7	-7	-7	-10	-7[1], -10

Package[3], [4]	**Area (mm)**	**Maximum User I/Os**					
QFN Packages (QF): Quad, flat, no-lead (0.5mm lead spacing)							
QFG32[4]	5 x 5	21					
QFG48[4]	7 x 7		37				
VQFP Packages (VQ): Very thin QFP (VQ44: 0.8mm lead spacing, VQ100: 0.5mm lead spacing)							
VQG44	12 x 12	33	33				
VQG100	16 x 16		64	80	80		
Chip Scale Packages (CP): Wire-bond, chip-scale, BGA (0.5mm ball spacing)							
CPG56	6 x 6	33	45				
CPG132	8 x 8			100	106		
TQFP Packages (TQ): Thin QFP (0.5mm lead spacing)							
TQG100	16 x 16						
TQG144	22 x 22			100	118	118	
PQFP Packages (PQ): Wire-bond, plastic, QFP (0.5 mm lead spacing)							
PQG208	30.6 x 30.6 mm				173	173	173
FBGA Packages (FT): Wire-bond, fine-pitch, thin BGA (1.0 mm ball spacing)							
FTG256	17 x 17 mm				184	212	212
FBGA Packages (FG): Wire-bond, fine-pitch, BGA (1.0 mm ball spacing)							
FGG324	23 x 23 mm					240	270

Notes:
1. -7 speed grade is only available in FT(G)256 package.
2. All packages are available in Pb-Free and RoHS6 compliant versions.
3. Area dimensions for lead-frame product are inclusive of the leads.
4. Only available in RoHS6 compliant and Halogen-free packages.

Zynq®-7000 Family Speed Grades

		Device Name[1]									
	Speed Grade	Z-7007S	Z-7012S	Z-7014S	Z-7010	Z-7015	Z-7020	Z-7030	Z-7035	Z-7045	Z-7100
C	-1	●	●	●	●	●	●	●	●	●	●
E	-2	●	●	●	●	●	●	●	●	●	●
	-3	–	–	–	●	●	●	●	●	●	–
I	-1	●	●	●	●	●	●	●	●	●	●
	-2	●	●	●	●	●	●	●	●	●	●
	-1L	–	–	–	●	●	●	–	–	–	–
	-2L	–	–	–	–	–	–	●	●	●	●

Notes:
1. For full part number details, see the Ordering Information section in DS190, *Zynq®-7000 All Programmable SoC Overview*.

- ● Available
- – Not offered

C = Commercial (Tj = 0°C to +85°C)
E = Extended (Tj = 0°C to +100°C)
I = Industrial (Tj = –40°C to +100°C)

Artix-7 FPGA Speed Grades

		Device Name[1]							
	Speed Grade	XC7A12T	XC7A15T	XC7A25T	XC7A35T	XC7A50T	XC7A75T	XC7A100T	XC7A200T
C	-1	•	•	•	•	•	•	•	•
	-2	•	•	•	•	•	•	•	•
E	-2L	•	•	•	•	•	•	•	•
	-3	•	•	•	•	•	•	•	•
I	-1	•	•	•	•	•	•	•	•
	-1L	•	•	•	•	•	•	•	•
	-2	•	•	•	•	•	•	•	•

Notes:
1. For full part number details, see the Ordering Information section in DS180, *7 Series FPGAs Overview*.

- • Available
- – Not offered

C = Commercial (Tj = 0°C to +85°C)
E = Extended (Tj = 0°C to +100°C)
I = Industrial (Tj = –40°C to +100°C)

Spartan-7 FPGA Speed Grades

		Device Name[1]					
	Speed Grade	XC7S6	XC7S15	XC7S25	XC7S50	XC7S75	XC7S100
C	-1	•	•	•	•	•	•
	-2	•	•	•	•	•	•
I	-1	•	•	•	•	•	•
	-2	•	•	•	•	•	•
	-1L	•	•	•	•	•	•
Q	-1	•	•	•	•	•	•

Notes:
1. For full part number details, see the Ordering Information section in DS180, *7 Series FPGAs Overview*.

- • Available
- – Not offered

C = Commercial (Tj = 0°C to +85°C)
I = Industrial (Tj = –40°C to +100°C)
Q = Expanded (Tj = –40°C to 125°C)

Spartan-6 FPGA Speed Grades

		Device Name[1]												
	Speed Grade	XC6SLX4	XC6SLX9	XC6SLX16	XC6SLX25	XC6SLX45	XC6SLX75	XC6SLX100	XC6SLX150	XC6SLX25T	XC6SLX45T	XC6SLX75T	XC6SLX100T	XC6SLX150T
C	-1L	•	•	•	•	•	•	•	•	—	—	—	—	—
	-2	•	•	•	•	•	•	•	•	•	•	•	•	•
	-3	•	•	•	•	•	•	•	•	•	•	•	•	•
	-3N	•	•	•	•	•	•	•	•	•	•	•	•	•
I	-1L	•	•	•	•	•	•	•	•	—	—	—	—	—
	-2	•	•	•	•	•	•	•	•	•	•	•	•	•
	-3	•	•	•	•	•	•	•	•	•	•	•	•	•
	-3N	•	•	•	•	•	•	•	•	•	•	•	•	•

Notes:
1. For full part number details, see the Ordering Information section in DS160, *Spartan-6 Family Overview*.

C = Commercial (Tj = 0°C to +85°C)
I = Industrial (Tj = –40°C to +100°C)

- • Available
- – Not offered

Device Ordering Information

ZYNQ

XC	7	Z	###	S	-1	FF	V	###	C
Xilinx Commercial	Generation	Family	Value Index	Single Core Indicator (Z-7007S, Z-7012S, Z-7014S)	Speed Grade -1: Slowest -L1: Low Power -2: Mid -L2: Low Power -3: Fastest	Package Type CL: Wire-bond (.8mm) SB: Bare-die Flip-chip (.8mm) FB: Bare-die Flip-chip (1mm) FF: Flip-chip (1mm)	V: RoHS 6/6 G (CLG) = RoHS 6/6 G (SBG, FBG, FFG) = RoHS 6/6 with exemption 15	Package Pin Count	Temperature Grade (C, E, I)

ARTIX 7

XC	7	A	###	-1	FF	G	900	C
Xilinx Commercial	Generation	Family	Logic Cells In 1K units	Speed Grade -1 = Slowest -L1 = Low Power -L2 = Low Power -2 = Mid -3 = Highest	Package Type CP: Wire-bond (.5mm) CS: Wire-bond (.8mm) SB: Bare-die Flip-chip (.8mm) FT: Wire-bond (1mm) FG: Wire-bond (1mm) FB: Bare-die Flip-chip (1mm) FF: Flip-chip (1mm)	V: RoHS 6/6 G: RoHS 6/6 w/exemption 15	Nominal Package Pin Count	Temperature Grade (C, E, I)

SPARTAN 7

XC	7	S	###	-1	FG	G	A	484	C
Xilinx Commercial	Generation	Family	Logic Cells In 1K units	Speed Grade -1 = Slowest -L1 = Low Power -2 = Mid	Package Type CP: Wire-bond (.5mm) CS: Wire-bond (.8mm) FG: Wire-bond (1mm) FT: Wire-bond (1mm)	G: RoHS 6/6	Package Designator	Package Pin Count	Temperature Grade (C, I, Q)

SPARTAN 6

XC	6	S	LX LXT	###	-1	FB	G	900	C
Xilinx Commercial	Generation	Family	Sub-families	Logic Cells In 1K units	Speed Grade -L1 = Low Power -2 = Mid -3 = Highest -N3 = No MCB functionality	Package Type CP: Wire-bond (.5mm) TQ: Quad Flat Pack (.5mm) CS: Wire-bond (.8mm) FT: Wire-bond (1mm) FG: Wire-bond (1mm)	G: RoHS 6/6	Package Pin Count	Temperature Grade (C, I)

Notes:
-L1 is the ordering code for the lower power, -1L speed grade.
-L2 is the ordering code for the lower power, -2L speed grade.
C = Commercial (Tj = 0°C to +85°C) E = Extended (Tj = 0°C to +100°C) I = Industrial (Tj = –40°C to +100°C) Q = Expanded (Tj = –40°C to +125°C)

Important: Verify all data in this document with the device data sheets found at www.xilinx.com

CPLD Ordering Information

XC2C128	-4	TQ	G	144	C
Device	Speed Grade -4 thru -10 (Fastest to Slowest)	Package Type QFN Packages (QF): Quad, flat, no-lead (0.5mm lead spacing) VQFP Packages (VQ): Very thin QFP (VQ44: 0.8mm lead spacing, VQ100: 0.5mm lead spacing) Chip Scale Packages (CP): Wire-bond, chip-scale, BGA (0.5mm ball spacing) TQFP Packages (TQ): Thin QFP (0.5mm lead spacing) FBGA Packages (FG): Wire-bond, fine-pitch, BGA (1.0mm ball spacing) FBGA Packages (FT): Wire-bond, fine-pitch, thin BGA (1.0mm ball spacing)	Pb-Free	Pin Count	Temperature Grade (C, I)

Notes:

C = Commercial (T_A = 0°C to +70°C) I = Industrial (T_A = –40°C to +85°C)

Important: Verify all data in this document with the device data sheets found at www.xilinx.com

Zynq®-7000 Device Footprint Compatibility

HR I/O, PS I/O, and GTP Transceivers

13mm–35mm

PCB Footprint Dimensions (mm)	13x13	17x17	19x19	19x19	23x23	27x27	27x27	31x31	35x35
Unique Footprint	CLG225	CLG400	CLG484	CLG485	FBG484	FBG676	FFG676	FFG900	FFG1156
Z-7007S	54, 84, 0	100, 128, 0							
Z-7012S				150, 128, 4					
Z-7014S		125, 128, 0	200, 128, 0						
Z-7010	54, 84, 0	100, 128, 0							
Z-7015				150, 128, 4					
Z-7020		125, 128, 0	200, 128, 0						
Mid-Range Devices (provided for reference) *HR I/O, HP I/O, PS I/O, GTX Transceivers*									
Z-7030				*50, 100, 128, 4*	*100, 63, 128, 4*	*100, 150, 128, 4*	*100, 150, 128, 4*		
Z-7035						*100, 150, 128, 8*	*100, 150, 128, 8*	*212, 150, 128, 16*	
Z-7045						*100, 150, 128, 8*	*100, 150, 128, 8*	*212, 150, 128, 16*	
Z-7100								*212, 150, 128, 16*	*250, 150, 128, 16*

The footprint compatibility range is indicated by shading per column.

Important: Verify all data in this document with the device data sheets found at www.xilinx.com

Artix®-7 Device Footprint Compatibility

HR I/O, GTP Transceivers

10mm–35mm

PCB Footprint Dimensions (mm)	10x10	10x10	15x15	15x15	17x17	19x19	23x23	23x23	27x27	27x27	35x35
Unique Footprint	CPG236	CPG238	CSG324	CSG325	FTG256	SBG484	FBG484	FGG484	FBG676	FGG676	FFG1156
XC7A12T		112, 2		150, 2							
XC7A15T	106, 2		210, 0	150, 4	170, 0			250, 4			
XC7A25T		112, 2		150, 4							
XC7A35T	106, 2		210, 0	150, 4	170, 0			250, 4			
XC7A50T	106, 2		210, 0	150, 4	170, 0			250, 4			
XC7A75T			210, 0		170, 0			285, 4		300, 8	
XC7A100T			210, 0		170, 0			285, 4		300, 8	
XC7A200T						285, 4	285, 4		400, 8		500, 16

The footprint compatibility range is indicated by shading per column.

Important: Verify all data in this document with the device data sheets found at www.xilinx.com

Spartan®-7 Device Footprint Compatibility

HR I/O

8mm–27mm

PCB Footprint Dimensions (mm)	8x8	13x13	15x15	15x15	23x23	27x27
Unique Footprint	CPGA196	CSGA225	CSGA324	FTGB196	FGGA484	FGGA676
XC7S6	100	100		100		
XC7S15	100	100		100		
XC7S25		150	150	100		
XC7S50			210	100	250	
XC7S75					338	400
XC7S100					338	400

The footprint compatibility range is indicated by shading per column.

Spartan®-6 Device Footprint Compatibility

I/O, GTP Transceivers

8mm–31mm

Dimensions (mm)	8x8	13x13	15x15	17x17	19x19	20x20	23x23	27x27	31x31
Unique Footprint	CPG196	CSG225	CSG324	FTG256	CSG484	TQG144	FGG484	FGG676	FGG900
XC6SLX4	106, 0	132, 0				102, 0			
XC6SLX9	106, 0	160, 0	200, 0	186, 0		102, 0			
XC6SLX16	106, 0	160, 0	232, 0	186, 0					
XC6SLX25			226, 0	186, 0			266, 0		
XC6SLX45			218, 0		320, 0		316, 0	358, 0	
XC6SLX75					328, 0		280, 0	408, 0	
XC6SLX100					338, 0		326, 0	480, 0	
XC6SLX150					338, 0		338, 0	498, 0	576, 0

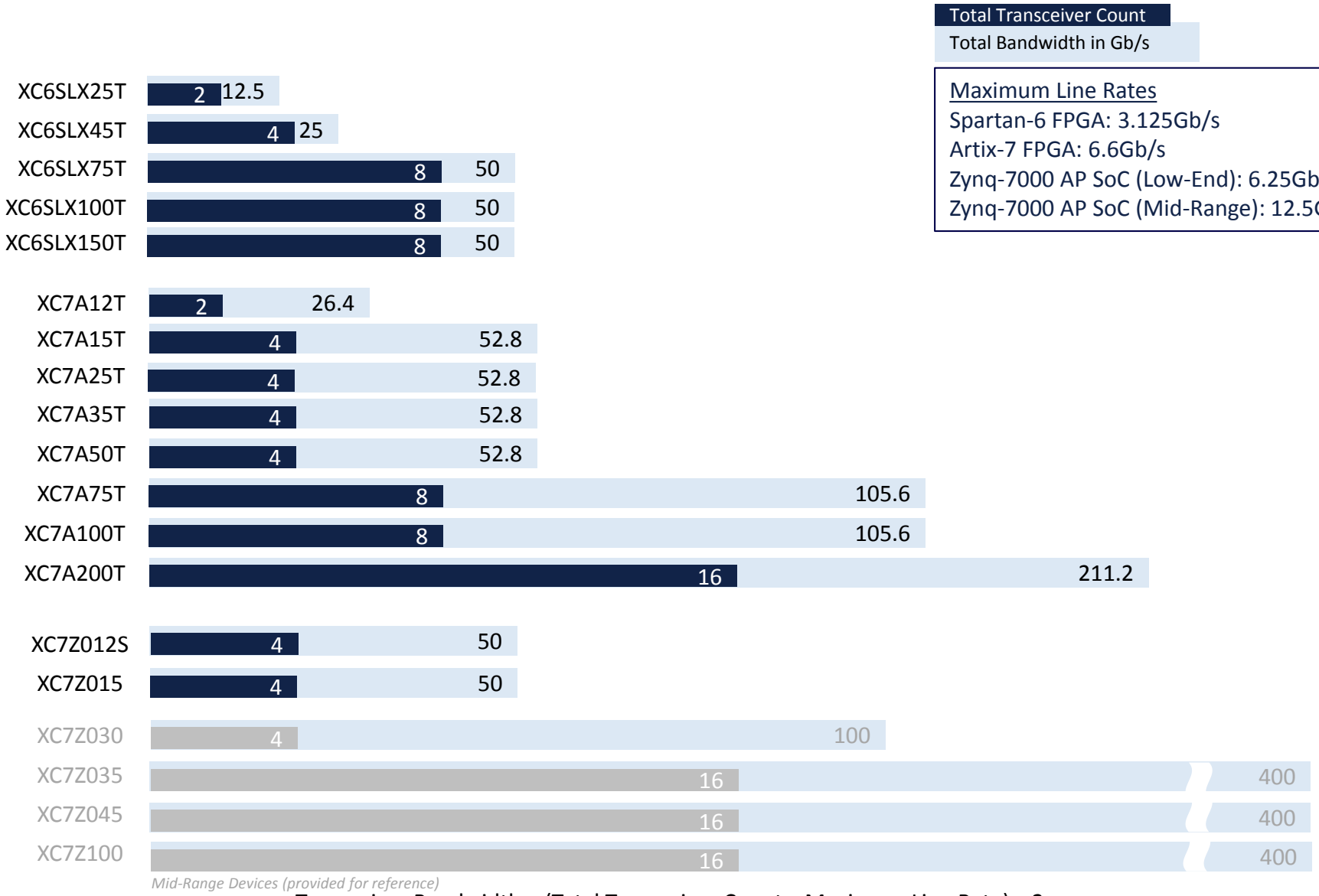
Dimensions (mm)			15x15		19x19		23x23	27x27	31x31
Unique Footprint			CSG324		CSG484		FGG484	FGG676	FGG900
XC6SLX25T			190, 2				250, 2		
XC6SLX45T			190, 4		296, 4		295, 4		
XC6SLX75T					292, 4		268, 4	348, 8	
XC6SLX100T					296, 4		296, 4	376, 8	498, 8
XC6SLX150T					296, 4		296, 4	396, 8	540, 8

The footprint compatibility range is indicated by shading per column.

Important: Verify all data in this document with the device data sheets found at www.xilinx.com

Transceiver Count and Bandwidth

SPARTAN-6 SPARTAN-7 ARTIX-7 ZYNQ



Maximum Line Rates
Spartan-6 FPGA: 3.125Gb/s
Artix-7 FPGA: 6.6Gb/s
Zynq-7000 AP SoC (Low-End): 6.25Gb/s
Zynq-7000 AP SoC (Mid-Range): 12.5Gb/s

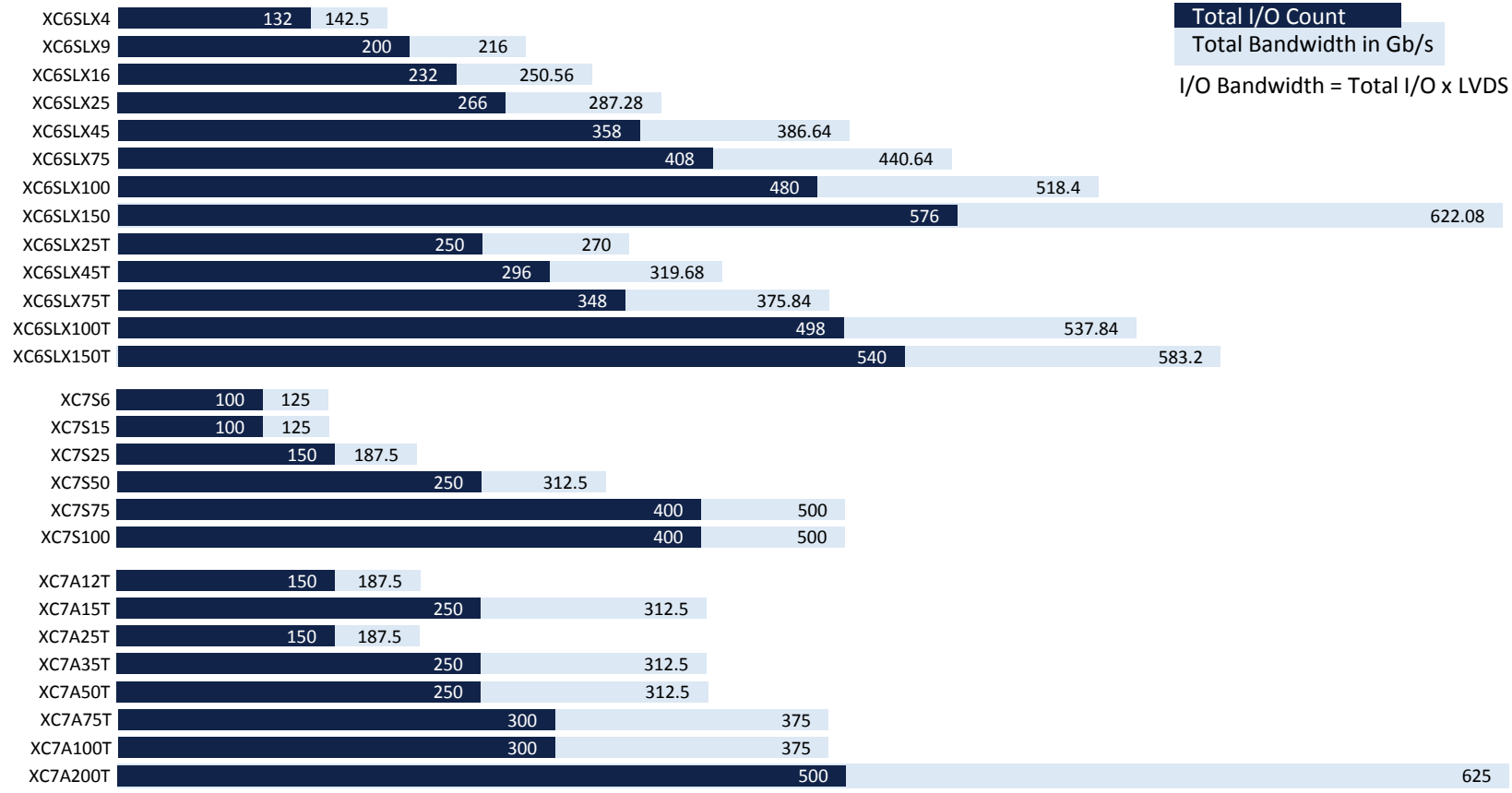
Mid-Range Devices (provided for reference)

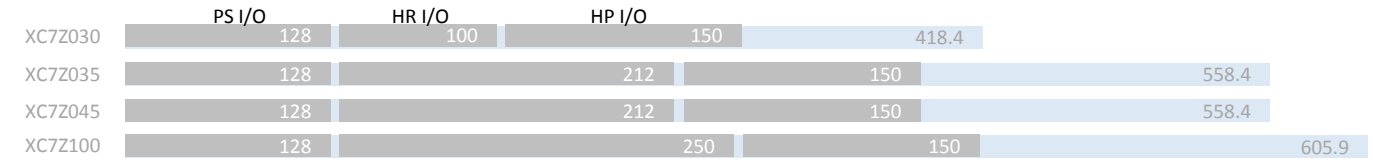
Transceiver Bandwidth = (Total Transceiver Count x Maximum Line Rate) x 2

Important: Verify all data in this document with the device data sheets found at www.xilinx.com

I/O Count and Bandwidth

SPARTAN-6 SPARTAN-7 ARTIX-7 ZYNQ





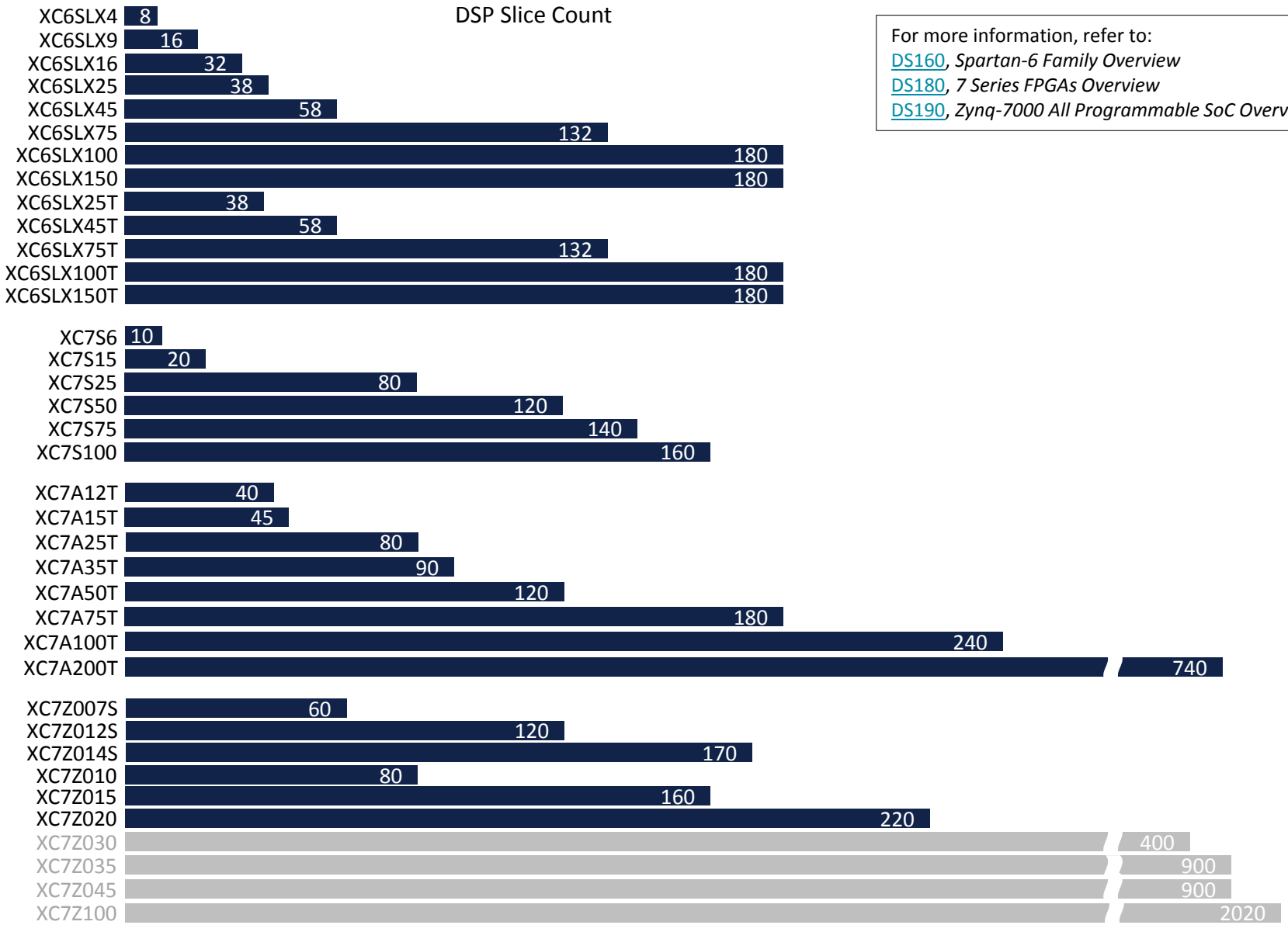
I/O Bandwidth =
(PS I/O x PS Bandwidth + HR I/O x HR LVDS Performance) + (HP I/O x HP LVDS Performance)

Zynq®-7000 AP SoCs: Dedicated DDR I/O bandwidth not included.

XILINX ALL PROGRAMMABLE

Digital Signal Processing Metrics

SPARTAN-6 SPARTAN-7 ARTIX-7 ZYNQ



For more information, refer to:
DS160, *Spartan-6 Family Overview*
DS180, *7 Series FPGAs Overview*
DS190, *Zynq-7000 All Programmable SoC Overview*

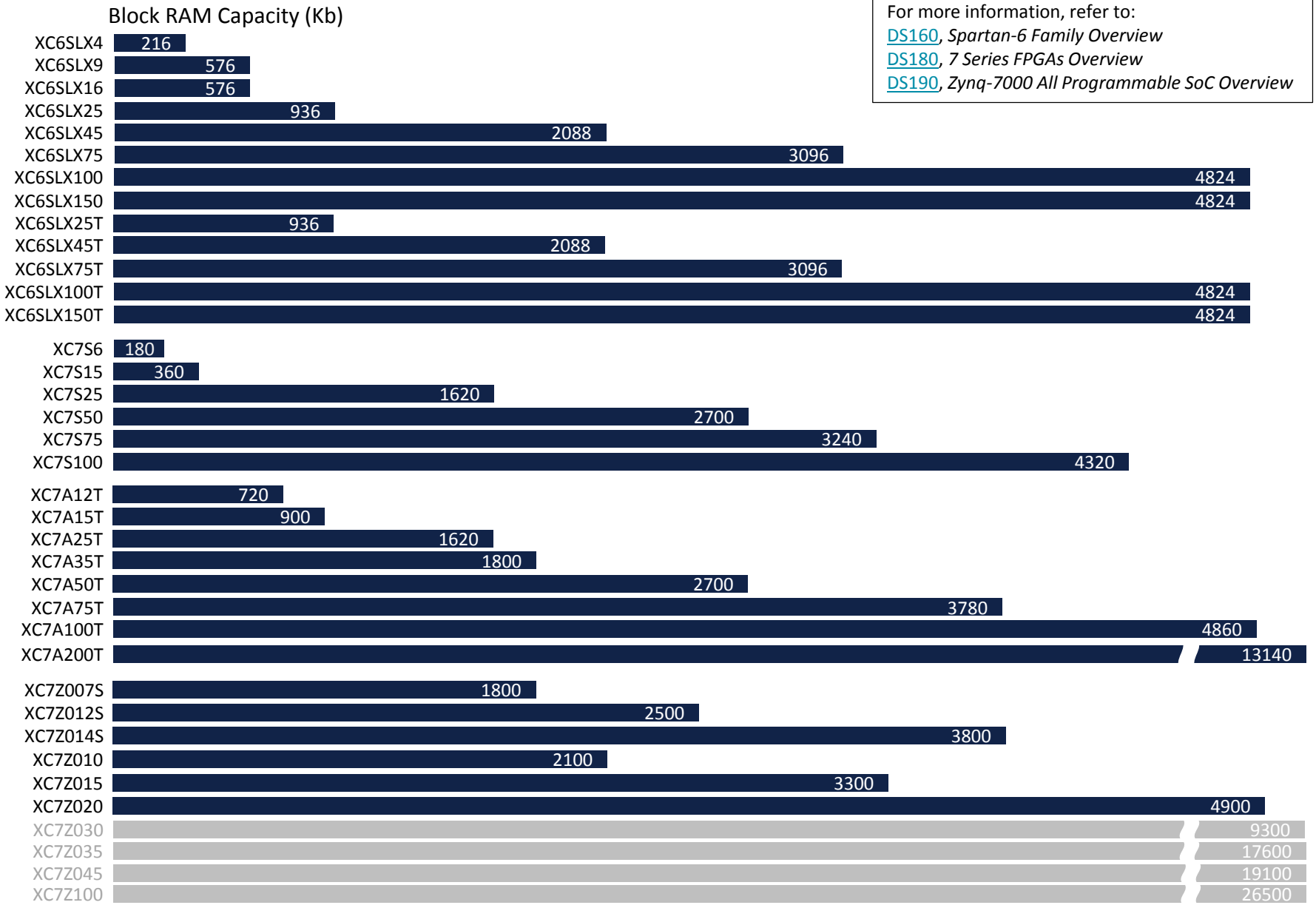
Important: Verify all data in this document with the device data sheets found at www.xilinx.com

XILINX ALL PROGRAMMABLE

Block RAM Metrics

SPARTAN-6 SPARTAN-7 ARTIX-7 ZYNQ

For more information, refer to:
DS160, *Spartan-6 Family Overview*
DS180, *7 Series FPGAs Overview*
DS190, *Zynq-7000 All Programmable SoC Overview*

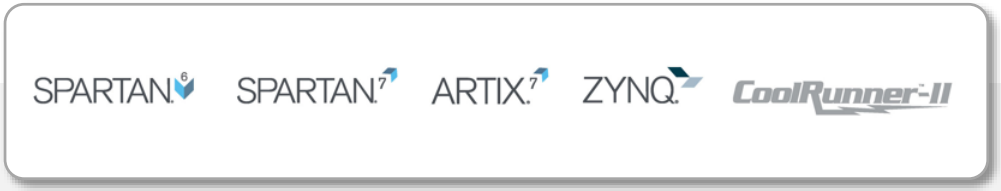


Mid-Range Devices (provided for reference)

Important: Verify all data in this document with the device data sheets found at www.xilinx.com

XILINX ALL PROGRAMMABLE

References



Spartan®-6 FPGA Product Page

DS160, *Spartan-6 Family Overview*

DS162, *Spartan-6 FPGA Data Sheet: DC and Switching Characteristics*

Spartan-7 FPGA Product Page

DS180, *7 Series FPGAs Overview*

DS189, *Spartan-7 FPGAs Data Sheet: DC and AC Switching Characteristics*

Artix®-7 FPGA Product Page

DS180, *7 Series FPGAs Overview*

DS181, *Artix®-7 FPGAs Data Sheet: DC and Switching Characteristics*

Zynq®-7000 SoC Product Page

DS190, *Zynq-7000 All Programmable SoC Overview*

DS187, *Zynq-7000 All Programmable SoC (Z-7007S, Z-7012S, Z-7014S, Z-7010, Z-7015, and Z-7020): DC and AC Switching Characteristics*

CoolRunner™-II CPLD Product Page

DS090, *CoolRunner-II CPLD Family Data Sheet*

Important: Verify all data in this document with the device data sheets found at www.xilinx.com